What is claimed is:

1. An integrated circuit device to be connected externally with a peripheral device operated by a first clock signal of a predetermined frequency, comprising:

a CPU having information on the frequency of the first clock signal;

a clock generator generating a second clock signal for operating the CPU and outputting a plurality of third clock signals obtained by dividing the frequency of the second clock signal;

a clock halt portion receiving the third clock signals from the clock generator and selectively outputting only one of the third clock signals according to the information from the CPU;

a timer activated only when receiving the one of the third clock signals from the clock halt portion and converting the frequency of the received clock signal for output; and

a clock synchronization serial port receiving the clock signal outputted from the timer and one of the other third clock signal(s) from the clock generator, and supplying either one of the received clock signals to the peripheral device according to the information from the CPU.

2. An integrated circuit device as claimed in Claim 1, wherein the clock generator includes a 1/n counter.

3. An integrated circuit device as claimed in Claim 1, wherein

the clock synchronization serial port includes a clock selector.

4. An integrated circuit device as claimed in Claim 1, wherein the timer receives a disable signal according to the information from the CPU and is deactivated by the disable signal.

5. An integrated circuit device to be connected externally with a peripheral device operated by a first clock signal of a predetermined frequency, comprising:

a CPU having information on the frequency of the first clock signal;

a clock generator generating a second clock signal for operating the CPU and outputting a plurality of third clock signals obtained by dividing the frequency of the second clock signal;

a clock halt portion receiving the third clock signals from the clock generator and selectively outputting only one of the third clock signals according to the information from the CPU;

a first and second timers individually activated only when receiving a respective one of the third clock signals from the clock halt portion and converting the frequency of the received clock signal for output; and

a clock synchronization serial port receiving the respective clock signals from the first and second timers, and supplying either one of the received clock signals to the peripheral device according to the information from the CPU.

6. An integrated circuit device as claimed in Claim 5, wherein the clock generator includes a 1/n counter.

7. An integrated circuit device as claimed in Claim 5, wherein the clock synchronization serial port includes a clock selector.

8. An integrated circuit device as claimed in Claim 5, wherein the first and second timers receive a first and second disable signals according to the information from the CPU, respectively, and the first and second timers are respectively deactivated by the first and second disable signals.

9. An integrated circuit device to be connected externally with a peripheral device operated by a first clock signal of a predetermined frequency, comprising:

a CPU having information on the frequency of the first clock signal;

a clock generator generating and outputting a second clock signal for operating the CPU;

a frequency divider circuit receiving the second clock signal from the clock generator and outputting a plurality of third clock signals obtained by dividing the frequency of the second clock signal;

a clock halt portion receiving one of the third clock signals from the frequency divider circuit and outputting the received clock signal according to the information from the CPU;

a timer activated only when receiving the one of the third

clock signals from the clock halt portion and converting the frequency of the received clock signal for output; and

a clock synchronization serial port receiving the clock signal outputted from the timer and the third clock signals from the frequency divider circuit, and supplying one of the received clock signals to the peripheral device according to the information from the CPU.

10. An integrated circuit device as claimed in Claim 9, wherein the clock synchronization serial port includes a clock selector.

11. An integrated circuit device as claimed in Claim 9, wherein the timer receives a disable signal according to the information from the CPU and is deactivated by the disable signal.

12. An integrated circuit device as claimed in Claim 9, further comprising:

another clock halt portion receiving a second clock signal from the clock generator and outputting the received clock signal according to the information from the CPU; and

another timer activated only when receiving the one of the second clock signals from the another clock halt portion and converting the frequency of the received clock signal for output;

wherein the clock synchronization serial port receives the clock signal outputted from the timer, the clock signal outputted from the another timer, the second clock signal received from the another clock halt portion and the third clock

signals from the frequency divider circuit, and supplies one of the received clock signals to the peripheral device according to the information from the CPU.